REMARKS

Applicants respectfully request reconsideration of the subject application, as amended. Claims 1-29 have been amended. Claim 30 is canceled. Accordingly, claims 1-29 are still pending in the application.

The Examiner has rejected claims 1-30 under 35 U.S.C. § 102(b) as being anticipated by Pockrandt (U.S. Patent 4,768,210). Applicants submit that Pockrandt discloses a method for the non-volatile storage of the counter including the successive storing of an actual counter reading into independent counter reading registers. Specifically, main register 8 and background register 9 are shown in Figure 1 of Pockrandt.

Applicants submit that the amended claims clearly claim a volatile and non-volatile values to generate a monotonic count value Pockrandt fails to disclose such features. Accordingly, Applicants submit that elements of the claimed embodiments are not disclosed in Pockrandt. Accordingly, Applicants submit that the amended claims distinguish over the relied upon Pockrandt reference and Applicants respectfully request the Examiner to withdraw the 35 U.S.C. § 102(b) rejection.

Accordingly, Applicants submit that amended claims 1-29 are in condition for allowance and solicit the Examiner for allowance of these claims.

Please charge any additional fees due, if any, to Deposit Account 02-2666.

Respectfully submitted,

BLAKELY SOKOLOFF TAYLOR & ZAFMAN LLP

Date: 12-11-02

William W. Kidd
Reg. No. 31,772

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025-1026
(512) 330-0844

VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A method comprising:

maintaining a first value for a first counter based on a content of a volatile memory;

maintaining a second value for a second counter based on a content of a non-volatile memory; and

controlling updates to the first value for the first counter and to the second value for the second counter, the first and second values used to generate a monotonic count.

2. (Amended) The method of claim 1, wherein the controlling comprises updating the second value for the second counter when the first value for the first counter meets a predetermined condition.

3. (Amended) The method of claim 1, comprising reading the first value for the first counter and the second value for the second counter,[;] wherein the controlling comprises updating the first value for the first counter in response to the reading of the [value for the first counter and the value for the second counter] monotonic count.

4. (Amended) The method of claim 1, wherein the controlling comprises updating the second value [for the second counter] upon a power on reset.

5. (Amended) The method of claim 1, wherein the controlling comprises updating the second value [for the second counter by a number] by programming [that number of] a bit location[(s)] or locations in a flash memory.

6. (Amended) The method of claim 1, wherein the controlling comprises updating the second value [for the second counter] by updating a [first block of flash memory and updating a second block of flash memory when the first block of flash memory] a portion of a flash memory when another portion of the flash memory meets a predetermined condition.

7. (Amended) A method comprising:

reading a count value for a monotonic counter, the monotonic counter at least partially basing the count value on a content of a volatile memory and a non-volatile memory; and

updating the count value for the monotonic counter by [a number in response to the reading of the value for the monotonic counter] utilizing contents of the volatile memory for lesser significant bits of the count value and contents of the non-volatile memory for higher significant bits of the count value.

8. (Amended) The method of claim 7, wherein the updating the count value for the monotonic counter comprises updating a flash memory to update the non-volatile memory.

9. (Amended) A method comprising:

powering on a monotonic counter, the monotonic counter at least partially basing a count value on a content of a volatile memory and a non-volatile memory; and

updating the count value for the monotonic counter on the powering on condition by [a number in response to the powering on of the monotonic counter] utilizing contents of the volatile memory for lesser significant bits of the count value and contents of the non-volatile memory for higher significant bits of the count value.

10. The method of claim 9, wherein the updating the count value for the monotonic counter comprises updating a flash memory to update the non-volatile memory.

11. (Amended) An apparatus comprising:

a [first] volatile counter to maintain a first value;

a [second] non-volatile counter to maintain a second value based on a content of a non-volatile memory; and

control logic to control updating the first and second values to control a monotonic count, the volatile counter to generate lesser significant bits of the monotonic count and the non-volatile counter to generate higher significant bits of the monotonic count.

12. (Amended) The apparatus of claim 11, wherein the control logic controls the [first] volatile counter to update the first value when the first and second values are read.

13. (Amended) The apparatus of claim 11, wherein the control logic controls the [second] non-volatile counter to update the second value when the [first] volatile counter meets a predetermined condition.

14. (Amended) The apparatus of claim 11, wherein the control logic controls the [second] non-volatile counter to update the second value upon a power on reset.

15. (Amended) The apparatus of claim 11, wherein the non-volatile memory comprises a flash memory[;] and wherein the control logic [controls programming] to program a number of bit location[(s)] or locations in the flash memory to update the second value.

16. (Amended) The apparatus of claim 11, wherein the non-volatile memory [comprises a first] is separated into more than one block of flash memory [and a second block of flash memory; and

wherein the control logic controls updating the first block of flash memory and updating the second block of flash memory when the first block of flash memory meets a predetermined condition], wherein individual blocks of flash memory are arranged to provide cascading of selective number of the higher significant bits of the monotonic count.

17. (Amended) An apparatus comprising:

a volatile memory to maintain a first value for a first counter;

a non-volatile memory to maintain a second value for a second counter; and

circuitry to maintain a count value for a monotonic counter, the circuitry to base the count value at least partially on [a content of] the first value for lesser significant bits of the count value and [non-volatile memory] the second value for higher significant bits of the

count value, and to update the count value by a number in response to a read of the count value for the monotonic counter.

18. (Amended) The apparatus of claim 17, wherein the non-volatile memory comprises a flash memory[;] and wherein the circuitry updates the count value by the number by programming [that number of bit location(s)] a bit location or locations in the flash memory.

19. (Amended) The apparatus of claim 17, wherein the non-volatile memory comprises a first block of flash memory and a second block of flash memory[;] and wherein the circuitry updates the [first block of flash memory by the number and updates the second block of flash memory if the first block of flash memory meets a predetermined condition] second block of flash memory and erases the first block of flash memory when a predetermined condition is met.

20. (Amended) An apparatus comprising:

a volatile memory to maintain a first value for a first counter;

a non-volatile memory to maintain a second value for a second counter; and

circuitry to maintain a count value for a monotonic counter, the circuitry to base the count value at least partially on [a content of] the first value for lesser significant bits of the count value and [non-volatile memory] the second value for higher significant bits of the count value, and to update the count value by a number in response to a powering on [of] condition for the circuitry.

21. (Amended) The apparatus of claim 20, wherein the non-volatile memory comprises a flash memory[;] and wherein the circuitry updates the count value by the number by programming [that number of bit location(s)] a bit location of locations in the flash memory.

22. (Amended) The apparatus of claim 20, wherein the non-volatile memory comprises a first block of flash memory and a second block of flash memory[;] and wherein the circuitry updates the [first block of flash memory by the number and updates the second block of flash memory if the first block of flash memory meets a predetermined condition] second block of flash memory and erases the first block of flash memory when a predetermined condition is met.

23. (Amended) An apparatus comprising:

one or more registers to store a first value;

a first adder to maintain the first value;

a flash memory to store a portion of bits used for a monotonic count;

one or more registers to store a second value;

a second adder to maintain the second value based on one or more programmed [bit] locations in the flash memory; and

a control engine to control the flash memory and the first and second adders, the first value used to determine lower significant bits of the monotonic count and the second value used to determine higher significant bits of the monotonic count, the lesser significant bits being volatile while higher significant bits being non-volatile.

24. (Amended) [An] The apparatus [comprising:

flash memory;

one or more registers to store a value;

an adder to maintain the value based on one or more programmed bit locations in the flash memory; and

a control engine to control the flash memory and the adder to update the value by a number in response to a read of the value] of claim 23, wherein the second value is updated when a predetermined condition is met in the one or more registers storing the first value.

25. (Amended) [An] The apparatus [comprising:

flash memory;

one or more registers to store a value;

an adder to maintain the value based on one or more programmed bit locations in the flash memory; and

a control engine to control the flash memory and the adder to update the value by a number upon] of claim 23, wherein the second value is updated when a power on reset condition occurs.

26. (Amended) A computer system comprising:

(a) a monotonic counter comprising:

(i) a [first] volatile counter to maintain a first value,

(ii) a [second] non-volatile counter to maintain a second value based on a content of a non-volatile memory, and

(iii) control logic to control updating the first and second values to control a monotonic count, the volatile counter to generate lesser significant bits of the monotonic count and the non-volatile counter to generate higher significant bits of the monotonic count; and

(b) one or more processors to read the first and second values.

27. (Amended) The computer system of claim 26, wherein the control logic controls the [first] volatile counter to update the first value when the first and second values are read.

28. (Amended) The computer system of claim 26, wherein the control logic controls the [second] non-volatile counter to update the second value when the [first] volatile counter meets a predetermined condition.

29. (Amended) The computer system of claim 26, wherein the control logic controls the [second] non-volatile counter to update the second value upon a power on reset of the monotonic counter.

Cancel claim 30.